21. The circuit arrangement of claim 20 wherein the controller includes a processor executing a program.

22. The circuit arrangement of claim 21 wherein M = 4.

23. The circuit arrangement of claim 20 wherein the predefined orientation is linear.

24. The method of claim 11 wherein bits in each group represents portion of a word.

REMARKS

This amendment is in response to the Office Action mailed September 6, 2002.

Before addressing the Office Action applicants summarize the actions taken on the claims filed in the application. Claims 1-10 are cancelled without prejudice. Newly added Claims 13-24 mirror the cancelled claims and are broader in several respects. However, the newly added claims identified applicants' invention in a clearer and more positive way. Claims 11 and 12 are amended as set forth above.

Referring now to the Office Action, the Examiner has cited U.S. Patent 6,313,932, Roberts et al., as the basic prior art reference. With respect to some of the claims (now cancelled) the Examiner argues that the Roberts reference

anticipates the claims. As to claims 11 and 12 and some of the cancelled claims, the Examiner combined the Roberts reference, as the basic teaching of applicants' invention, with other references that the Examiner deemed teach features of applicants' invention not disclosed in Roberts. Because applicants' invention is so different from the teachings of Roberts it is applicants' contention that the Roberts reference alone or combined with other references neither anticipate nor suggest applicants' invention. As a consequence applicants believe that by distinguishing the claims from Roberts the other references with which it is combined are merely cumulative and does not suggest applicants' invention.

Roberts reference (U.S. Patent 6,313,932) teaches an optical transmission system in which a detector array 8 (Fig. 4) detects data transmitted in optical signals. An alignment processor 40 receives the output signals from each of the detector elements 10, combines the output from adjoining pairs of the detector elements 10 and maps the output onto binary values of transmitted channels (column 8, lines 30-53). In contrast, applicants' invention as claimed includes an aligner which determines the misalignment between groups of bits and adjusts the groups of bits relative to one another to remove the misalignment therebetween. It is clear that the invention disclosed in Roberts is different from the invention disclosed in applicants' claim. In particular and in respect to the claims there is no teaching in Roberts or any of the secondary references that suggest determining misalignment between groups of transmitted data bits and adjusting them to compensate for this misalignment. Applicants direct the attention of the Examiner to page 26 of applicants' specification and Figure 12 where the problem is discussed and the solution is set forth.

Regarding a rejection under 35 USC 102, it is hornbook law that such a rejection can only be sustained if every element and function provided in the claims are present in a single reference. As pointed out above and stated, for example, in the aligner set forth in claim 13 this element is missing in Roberts. Therefore, none of applicants' claims are anticipated by Roberts.

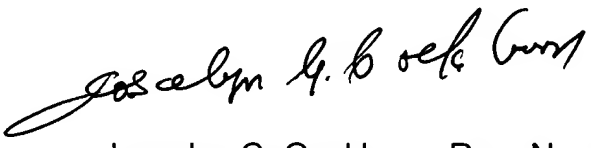
Regarding a rejection under 35 USC 103, the Examiner relied on Roberts as the primary reference and several other secondary patents to disclose features which according to the Examiner is not present in the Roberts reference. However, in light of the fact that applicants have distinguished the Roberts reference from the claimed invention and none of the secondary references provides the information which is lacking in the Roberts reference it is applicants' contention that none of the combined references would render any of the claims obvious. Therefore, the claims are patentable over the reference, under 35 USC 103.

Applicants reviewed the drawings and found minor errors in Figures 4, 5, 6, 8, 12, 13 and 14. Pending approval of the examiner, attached are the figures with changes marked in red for forwarding to the Official Draftsperson.

It is believed that the present invention answers all the issues raised by the examiner. Reconsideration is hereby requested and an early allowance of all the claims is solicited.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "Version with markings to show changes made".

Respectfully Submitted,



Joscelyn G. Cockburn, Reg. No. 27,069
Attorney of Record
Customer No. 25299

JGC:ko
Phone: 919-543-9036
FAX: 919-254-2649

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Page 1, Paragraph starting on Line 5 has been amended as follows:

The listed related patent applications are incorporated herein by reference:
Patent Application ~~RA998-037~~ (S/N 09/330,968 [ )], filed June 11, 1999, entitled: High Speed Parallel/Serial Link for Data Communication;
Patent Application ~~RA998-038~~ (S/N 09/330,735 [ )], filed June 11, 1999, entitled: System that Compensates for Variances Due to Process and Temperature Changes;
Patent Application ~~RA998-039~~ (S/N 09/330,713 [ )], filed June 11, 1999, entitled: Initialization System for Recovering Bits and Group of Bits from a Communications Channel;
Patent Application ~~RA999-033~~ (S/N 09/330,971 [ )], filed June 11, 1999, entitled: Low Differential Driver.

Page 8, Paragraph starting on Line 4 has been amended as follows:

Still referring to Figure 2, Parallel Data Streams D0-D3 are presented to the input of the Latches L1-L4. A system clock signal is also provided to each one of the latches. As stated previously, the interface from the module to the DASL is a parallel interface. Usually, the number of bits in the parallel interface is on a byte (8-bit) boundary. According to the present invention, it is more advantageous to partition the bits into nibbles for processing and sending through the serial link. In one embodiment of the present invention, 16-bit parallel data streams are supplied to DASL interface. The bit streams are partitioned into four groups of four bit (4 bits = 1 nibble) streams. Each of the nibbles is processed according to the teaching of the present invention

and is sent over a serial link. As a consequence, to transmit the 16-bit, four serial links would be required. Each nibble of data is processed in the same way; therefore, the description of one (set forth hereinafter) is intended to cover the processing of the others. The four parallel data bit streams are transformed into a high speed serial bit stream by latching each of the four bit streams in one of the Latch L1 through L4 and sequentially strobing the latched information at four time the parallel clock rate using Multiplexer Circuit 22. The data stream is then reshaped by serial Latch L5, which is clocked also at four times the parallel clock rate and sent into a low power Differential Driver D1.

Page 9, Paragraph starting on Line 23 has been amended as follows:

Still referring to Figure 2A, the latches L0, L1, L2 and L3 are driven by 125 nanosecond clock labelled OSC 125. MUXA and MUXB are driven by a clock labelled OS 125. This clock is similar to the one used to drive latches L0 through L3. With respect to MUXA and MUXB, when the clock phase is 0, the contents of the L3 latch is passed through MUXA and the L2 latch is passed through MUXB. When the clock phase is a 1, data from latch L1 passes through MUXA and the data from latch L0 passes through MUXB.

Page 10, Paragraph starting on Line 19 has been amended as follows:

Figure 3 shows a 2 to 1 multiplexer circuit. The 2 to 1 multiplexer (MUX) circuit is a basic building block which can be connected with other 2 to 1 circuits to provide the 4 to 1 Multiplexer Circuit 22 (Fig. [1] 2) or 32 to 1 MUX (Fig. 6). Such interconnection is within the skill of one skilled in the art and further details of interconnection will not be given. Still referring to Fig. 3, inputs are D0 and D1. The output is labelled Z. The control is furnished by Control Input SD. Transistors P select and N select are configured as an inverter that inverts the control input signal SD.

Similarly, Transistor PD1 and ND1 are inverters that invert the signal D1. Transistor PD0 and ND0 are connected as inverters to invert the signal D0. Both inverters provide inversion and buffering for their respective inputs, D0 and D1. Transistors PD0 gate and ND0 gate, PD1 gate and ND1 gate act as transmission [gate past] pass gate for these signals to the output Z. In operation, the select signal SD turns on either the pass gate [pass] for D0 or D1. This is supplied to the output through inverter/buffer comprising of Transistors POUT and NOUT.

Page 12, Paragraph starting on Line 2 has been amended as follows:

Current drawn by the driver is roughly 7.5 milliampere. Wattage drawn from the 1.5 volts supplied is 11.3 Mwatts, half of the power drawn from the more conventional driver having the same level of differential output swing as its driver. Additional wattage is incurred in either scheme due to driving on and off the capacitance of the transistors T1 through T4 to ground. Or in the case of the low power driver, current sent at the time of transition shoots through series devices T1, T2 (T3, T4). This can be minimized by using smaller devices and by increasing the device resistance of switches T1 through T4 into the range of 10 Ohms as mentioned above. This will limit additional wattage due to the transition to an additional 2 to 3 milliwatts. This circuit is particularly [importance] important for a switch application where 64 drivers are needed. The savings is approximately 2 watts/switch. The savings will mean financial savings for the switch module package, the box cooling and the size/cost of the power supply.

Page 13, Paragraph starting on Line 28 has been amended as follows:

Figure 6 shows a circuit diagram for the bit synchronization and nibble synchronization Circuit 22 (Fig. 5). To simplify the discussion, elements in Fig. 6 that are common with elements in Fig. 5 are labelled with the same numerals. The system

includes a 40 element delay line circuit 24. The delay line includes elements 00 through 39. The output from each stage of the delay line is connected to a latch in a set of 40 L1 latches labelled 26'. A gated 4 NSC clock is also coupled to the data latches 26'. Bits 08 through 39 of the L1 latches are connected to a 32 by 1 MUX28. A control signal labelled MUX2 is also connected to MUX28. As will be described subsequently, this control signal is generated by a microprocessor executing a program or from a state machine. The output from MUX28 is fed into L2 latch [34] 35. A line labelled Bit 2 is outputted from latch 34 and is fed into a 2 to 4 deserializer 32. The bit on the line represents one of the bits captured in the delay line. Four data bits are outputted on a bus labelled RCV DATA. As will be explained subsequently, these four bits are used to detect the nibble which was transmitted from the transmitter portion of the interface.

Page 14, Paragraph starting on Line15 has been amended as follows:

Still referring to Figure 6, Bits 00 through 31 of the 40 L1 latches are fed into 32 by 1 MUX30. A control signal labelled MUX1 is provided to the MUX30. The control signal, when activated, informs the MUX which one of the latched data should be passed. This control signal is generated by a program running in a processor or from state machine logic (to be discussed hereinafter). The output from MUX30 is fed into L2 Latch 38. The output from L2 Latch 38 is labelled Bit 1 and is fed into Deserializer 32. The bit on the line labelled Bit 1 represents the other bit captured in the delay line. With two bits captured, the four bit nibble can be easily generated. A four nanosecond B clock is also provided to L2 Latch [34] 35 and L2 Latch 38. Bits 0 through 39 of the 40 L1 latches are also fed into 40 L2 latches. A four nanosecond gated B clock is also fed into the 40 L2 latches. The output from the 40 L2 latches are used by Controller 34 to find edges within the input signal.

Page 20, Paragraph starting on Line 9 has been amended as follows:

If the program traverses Path A [into Block H], the pattern set forth in the Table II is observed. If the program exits along Path B, the pattern identified with B in Table II is observed. If the program exits along Path C, the pattern set forth with C in Table II is observed. If the program exits along Path C into the Error Block, this signifies an error condition in which the program loops and restarts the process. If the program exits along Path B, it enters the block labelled X0. In Block X0, it performs the function set forth under item 6, Table III. If the value calculated in X0 is a 1, this signifies that Initial Edge 1 is found (see Table IV). The program would then descend into the block labelled X1. In X1, the function performed is listed under item 20 of Table III. From Block X1, the program can exit along G or H. The function which is associated with G and H is set forth under the named letters in Table II. If the program exits along H, it enters the error block and the process is repeated as described above.

Page 21, Paragraph starting on Line 10 has been amended as follows:

It should be noted that in EQ2, 8 is subtracted because MUX28 carries bits 8 through 39 (Figure 6). It should also be noted that the control line MUX2, Fig. 6, equals Midbit 2. Similarly, control line MUX1 equals Midbit 1. Stated another way, once these values are determined, they are used for setting the MUX30 and MUX28 and only the contents of latches that have a value corresponding to these set values will be allowed to pass through MUX28 and MUX30 into L2 Latch 38 and L2 Latch 34. The output from Latch 38 becomes Bit 1, while the output from L2 Latch [34] 35 becomes Bit 2. The two bits are used to generate the nibble (4 bits) that were transmitted originally.

Page 22, Paragraph starting on Line 4 has been amended as follows:

To perform bit alignment, the received data is fed into a series of delay blocks D1 through D40, where the delayed data is oversampled and latched by latches L1 through L40. The captured oversampled data is then fed into a controller, which looks at the oversampled data to determine where in the series of latch positions did data transitions occur. This is done to determine two sample points in the stream of oversampled data with the highest probability of uncorrupted data. The oversampled data which as the least probability of data error is the oversampled data contained in the latches farthest away from the data transitions. This is because all high speed systems have data jitter in the form of the system clock jitter, data intersymbol and transmission media distortions as well as system cross talk that make the sample around data transitions uncertain as to data integrity. By averaging the positions determined to have transitioning data, the controller [than] then determines which of the latched data to be used for the serial data samples.

Page 25, Paragraph starting on Line 19 has been amended as follows:

Figure 15 shows a multibit port in Module A connected to a multibit port in Module B. Only the transmit and receiving portion of each module is shown. It should be understood that Module A also has Rx section and Module B has a Tx section which are not shown for purposes of simplicity. The Tx port of Module A includes a 16-bit register in which a parallel interface of bit streams is presented. The bit streams are grouped into groups of four (4), feed through a dedicated DASL transmitter (Tx) to dedicated drivers (DR). Each of the drivers forwards the high speed data stream through dedicated serial links labelled A, B, C and D. The high speed links A, B, C and D form a high speed bus that transmits data at very high transmission rates. On the receiving side, each receiver in a group of dedicated receivers receive data from a

dedicated link, passes the data to nibble recovery system which generates the transmitted four data streams and forwards them to Word Aligner 80. The function of Word Aligner 80 is to recover the word that was transmitted from the Tx port.

In the Claims:

Claims 1-10 have been canceled.

Claims 11 and 12 have been amended as follows:

11. (Amended) A method of processing data comprising the steps of:

receiving multiple streams of serial data;

generating from each one of the multiple stream of serial data a group of parallel bit streams;

storing in a computer memory [information] bit patterns representing different groups of parallel bit streams;

searching the memory with a programmed computer to detect a [predetermined] predefined bit pattern stored in each of said different groups; [and]

determining misalignment between predefined bit patterns; and

using said programmed computer and the misalignment to adjust the [predetermined] predefined bit pattern for all groups until said bit pattern is linearly aligned within said computer memory.

12. (Amended) The method of claim 11 wherein the [predetermined] predefined bit pattern includes 0101.

Claims 13-24 have been added.

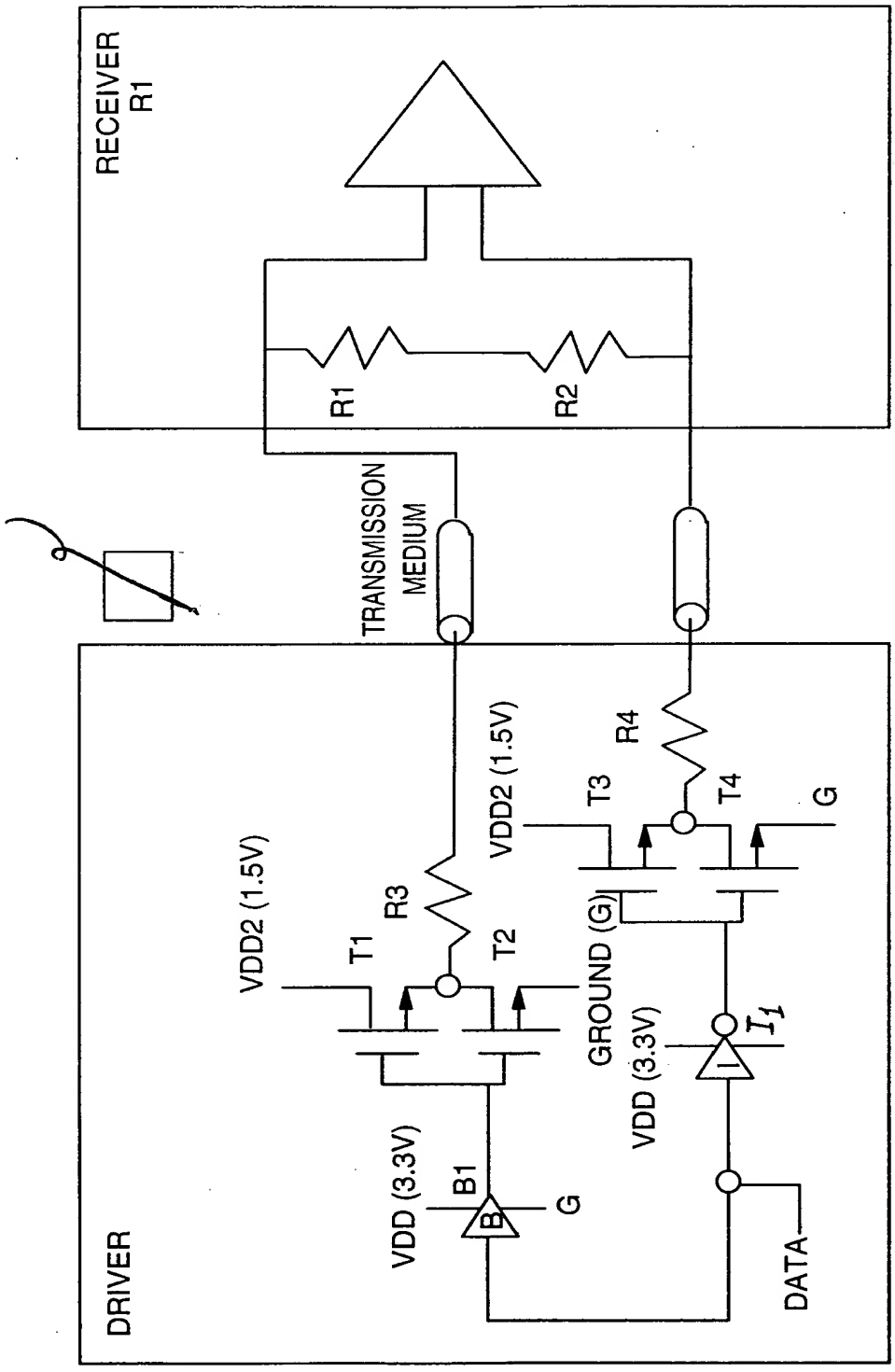


FIG. 4

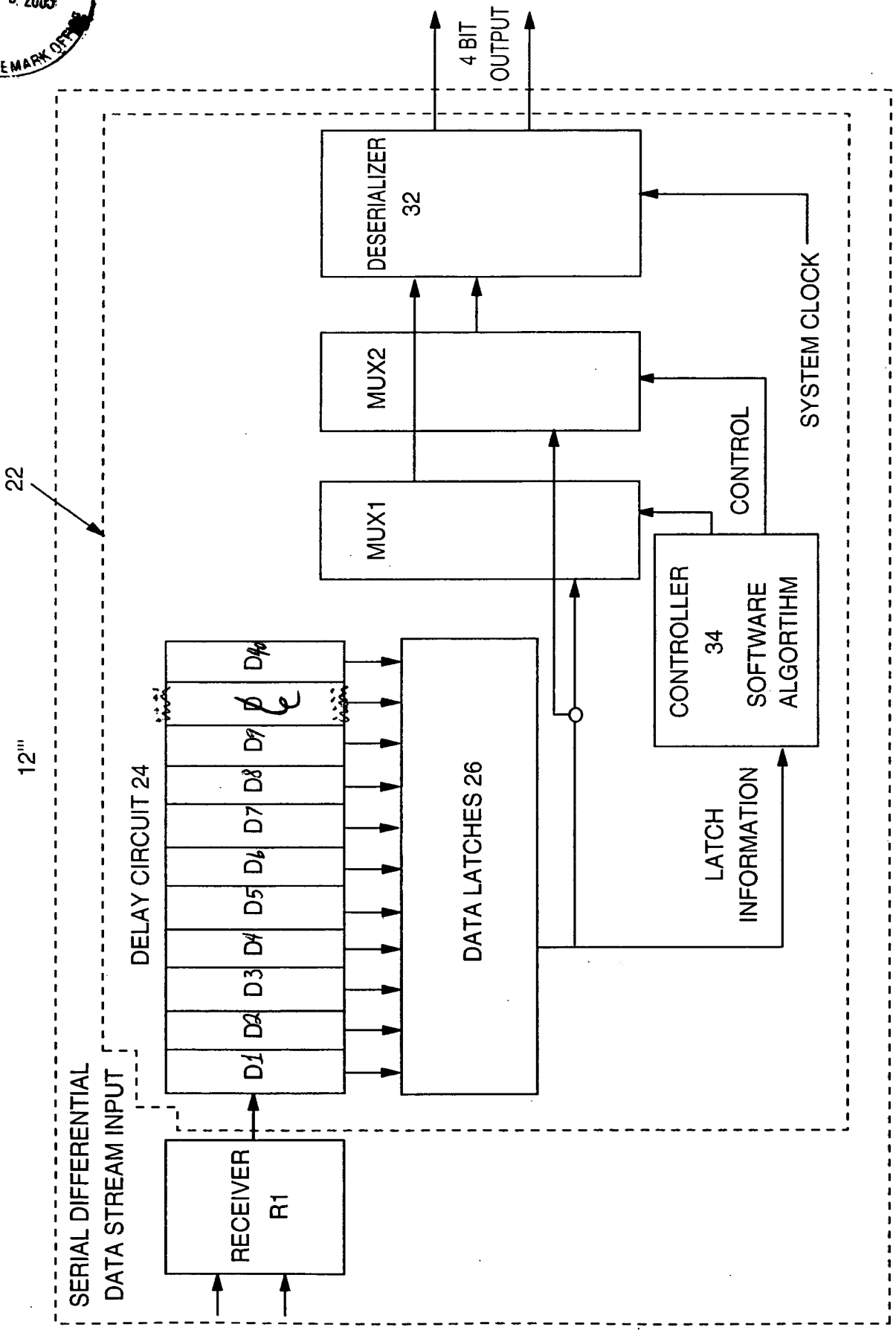


FIG. 5

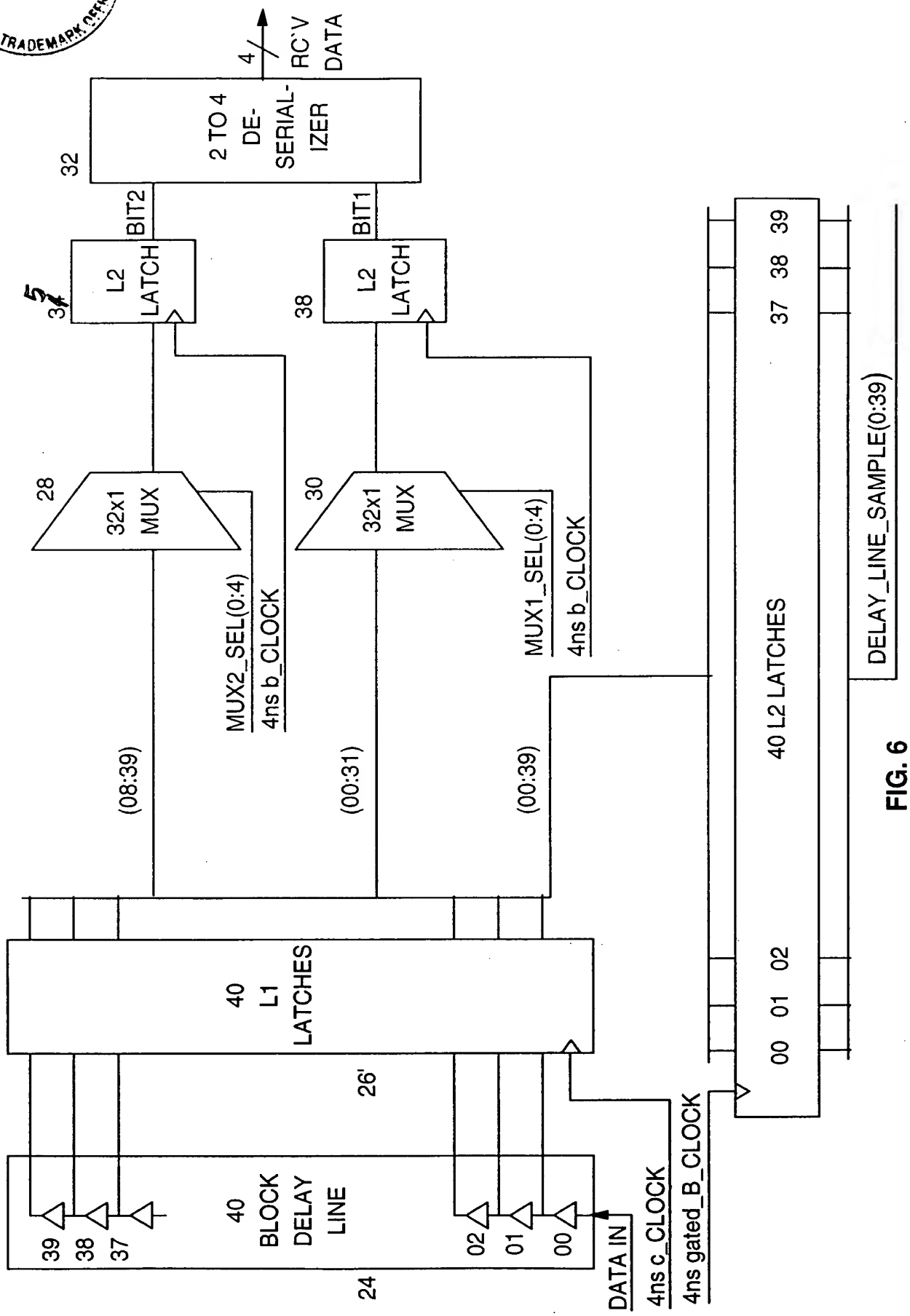


FIG. 6

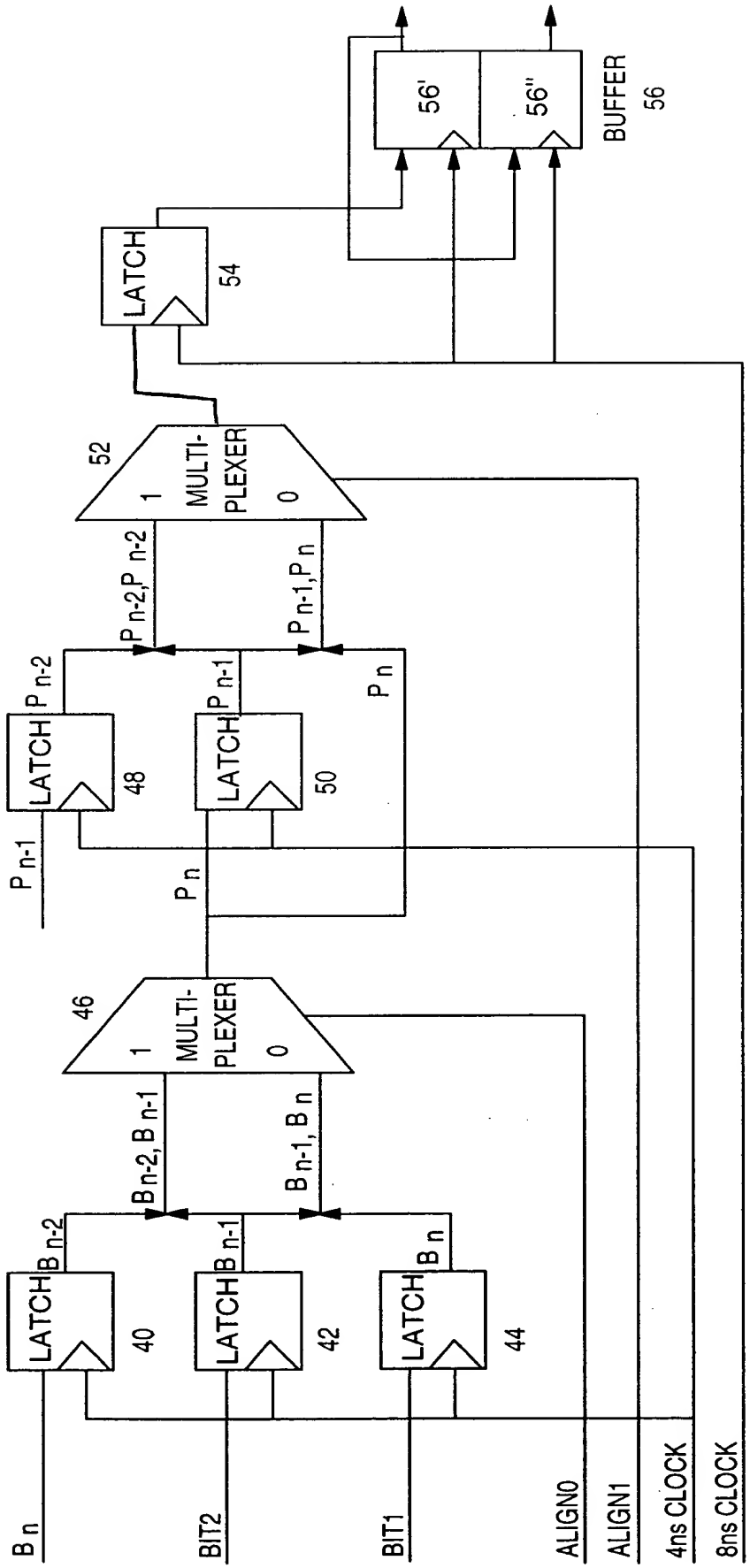


FIG. 8

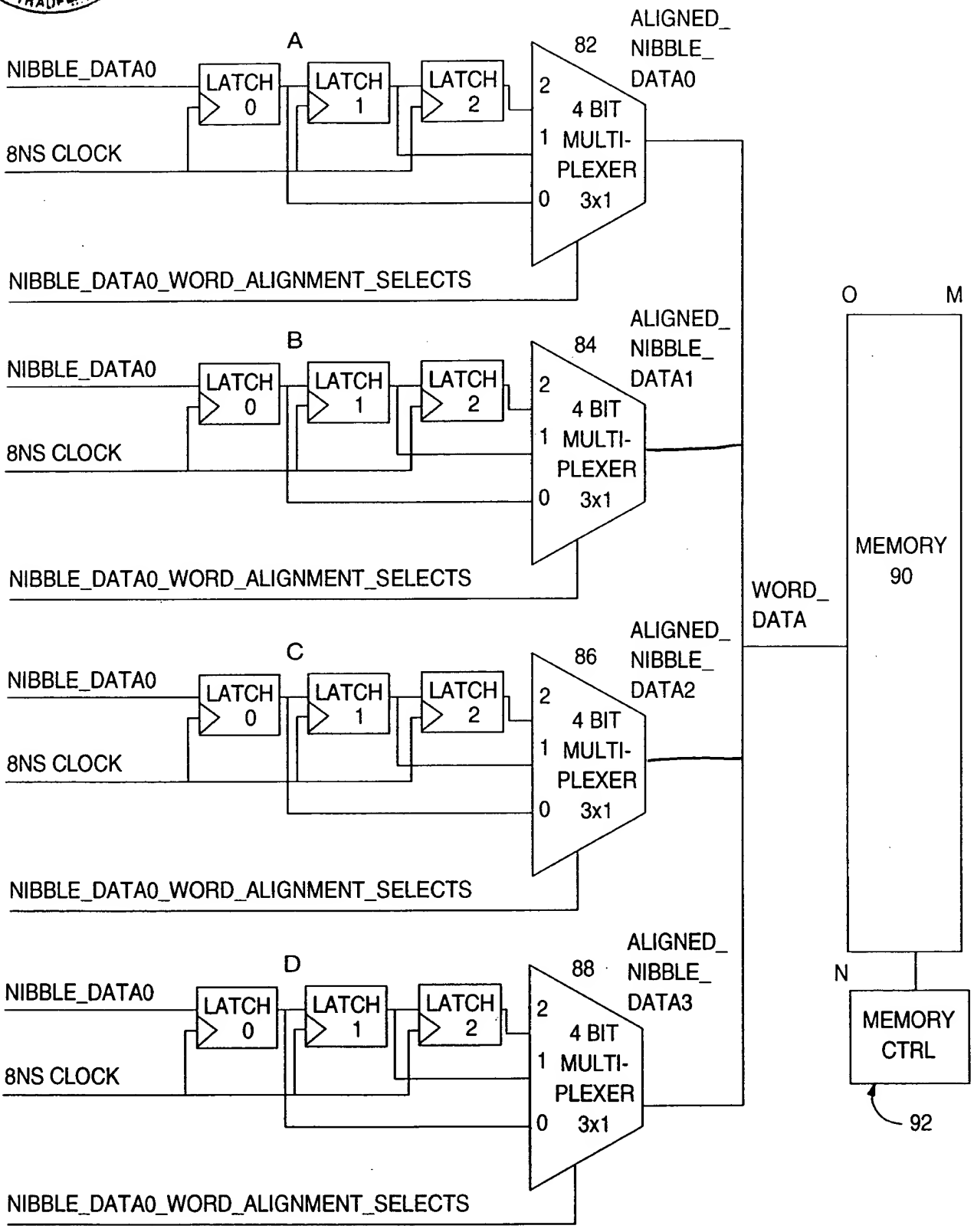


FIG. 12

SAMPLE MEMORY BUFFER ROW NUMBER	WORD DATA			
	NIBBLE 0	NIBBLE 1	NIBBLE 2	NIBBLE 3
1	A	A	A	A
2	A	A	A	A
3	A	A	A	A
4	A	5	A	A
5	5	5A	5	5A
6	A	A	A	~~A~~5
7	A	A	A	A
8	A	A	A	A
9	A	A	A	A
10	A	A	A	A
11	A	A	A	A
12	A	A	A	A
13	A	A	A	A
14	A	A	A	A
15	A	A	A	A
16	A	A	A	A
17	A	A	A	A
18	A	A	A	A
19	A	A	A	A
20	A	5	A	A

FIG. 13

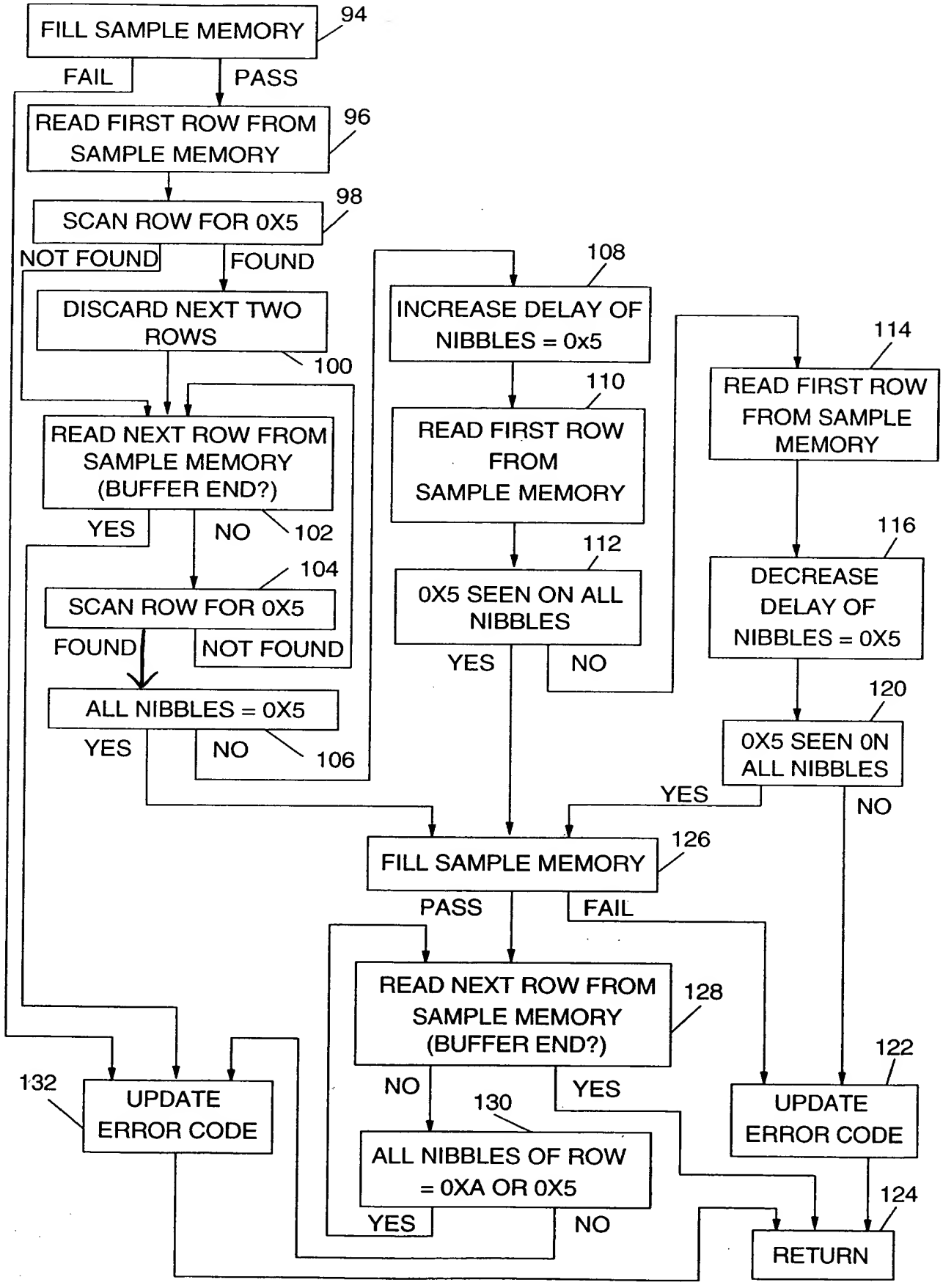


FIG. 14